**Cell Description:**

This is a standard two input XOR cell with the following Boolean equation.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "XOR2X1" "behavioral"

module XOR2X1 ( Y, A, B );

input A;

output Y;

input B;

xor(Y, A, B);

specify

(A => Y) = (1.0, 1.0);

(B => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| XOR2X1 | 27.0 | 12.0 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.309335 | 0.536119 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.337925 | 3.873978 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.249189 | 3.189955 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| XOR2X1 | 0.214332 | 3.063275 |

**Logic Symbol:**

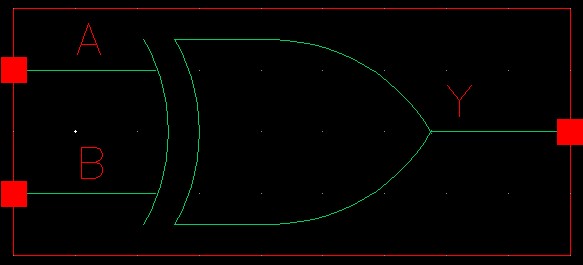
****

Figure : Symbol View for the XOR cell.

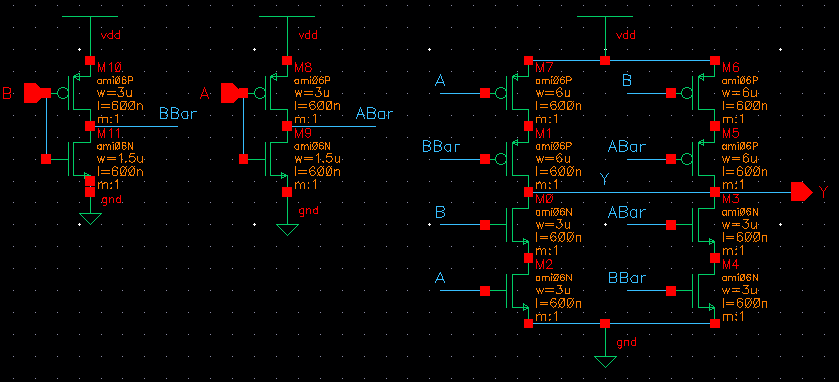
**CMOS Schematic:  
  
**

Figure : CMOS Schematic for the XOR2X1 cell.

**CMOS Layout:**

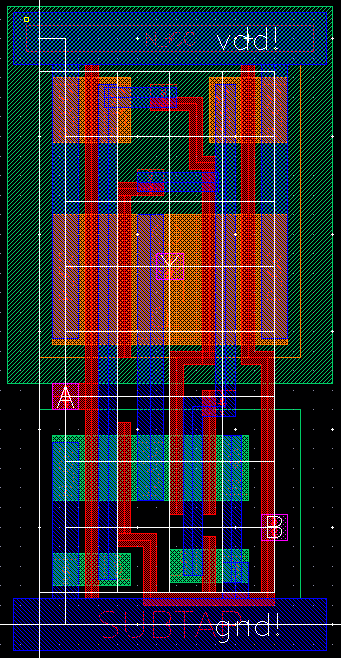
****

Figure : CMOS layout for the Nor2X1 cell.